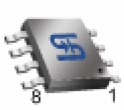
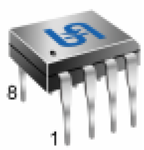
TS34063

Dc to Dc Converter Controller

SOP-8



DIP-8



Pin assignment:
1. SC
2. SE
3. CT
4. Gnd
5. Comp.
6. Vcc
7. Ipk
8. Vdriver

Supply Voltage Range 3 V to 40V
Output Driving Current 1.5A
Oscillator Frequency up to 100KHz

General Description

The TS34063 is a monolithic switching regulator and subsystem intended for use as DC to DC converter. It contains an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active peak current limit circuit, drive and a high current output switch.
The TS34063 is specifically designed to be incorporated in step-up, step-down and voltage inverting converter applications.
The TS34063 is offered in SOP-8 and DIP-8 package.

Features

- ✧ Power forward control circuit
- ✧ Operating voltage form 3V to 40V
- ✧ Low standby current
- ✧ Current limit adjustable
- ✧ Output switch current up to 1.5A
- ✧ Variable oscillator frequency up to 100KHz (max)
- ✧ Output voltage adjustable

Pin Descriptions

Name	Description
SC	Switch Collector
SE	Switch Emitter
CT	Timing Capacitor
Gnd	Ground
Comp.	Comparator Inverting Input
Vcc	Vcc Collector
Ipk	Ipk Sense
Vdriver	Driver

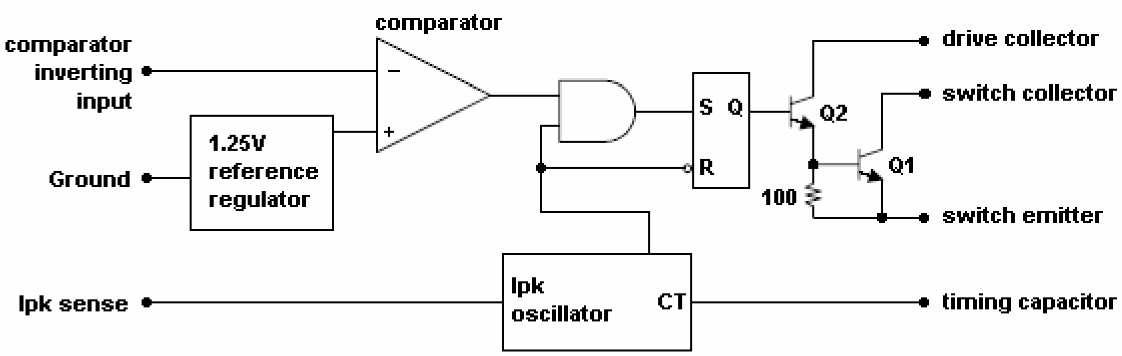
Applications

- ✧ Charger
- ✧ xD-ROM, xDSL product
- ✧ DC to DC converter s

Ordering Information

Part No.	Operating Temp. (Ambient)	Package
TS34063CD	-20 ~ +85 °C	DIP-8
TS34063CS		SOP-8

Block Diagram



Absolute Maximum Rating

Supply Voltage	V_{CC}	40	V
Comparator Input Voltage Range	V_{FB}	- 0.3 ~ 40	V
Switch Collector Output Voltage	$V_{C(SW)}$	40	V
Switch Emitter Voltage	$V_{E(SW)}$	40	V
Switch Collector to Emitter Voltage	$V_{CE(SW)}$	40	V
Driver Collector Voltage	Vc(driver)	40	V
Driver Collector Current (note 1)	Ic(driver)	100	mA
Output Switching Current	I_{SW}	1.5	A
Power Dissipation DIP-8 SOP-8	Pd	1.0 0.5	W
Operating Junction Temperature Range	T_J	-0 ~ +125	^oC
Storage Temperature Range	T_{STG}	-65 ~ +150	^oC

Note: Maximum package power dissipation limits must be observed

Electrical Characteristics (V_{CC} =5V, Ta =25 ^oC; unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator (OSC)						
Frequency	F_{OSC}	C_T = 1nF, Vpin5= 0V	24	33	42	KHz
Charge Current	I_{CHARGE}	V_{CC} = 5V ~ 40V	--	30	--	uA
Discharge Current	$I_{DISCHARGE}$	V_{CC} = 5V ~ 40V	--	200	--	uA
Discharge to Charge current ratio	$I_{DISCHARGE}$ / I_{CHARGE}	Pin7 to Vcc	--	6.5	--	--
Current Limit Sense Voltage	$V_{IPK(SENSE)}$	$I_{DISCHARGE}$ = I_{CHARGE}	250	--	350	mV
Output switch (note1)						
Saturation Voltage	$V_{CE(SAT)}$	I_{SW}= 1A, pin1,8 connected)	--	1.0	1.3	V
Saturation Voltage	$V_{CE(SAT)}$	I_{SW}= 1A, Id=50mA	--	0.45	0.7	V
DC current gain	H_{FE}	I_{SW} = 1A, Vce= 0.5V	--	75	--	--
Collector off-state current	$I_{C(OFF)}$	Vce= 40V	--	0.01	100	uA
Comparator						
Threshold Voltae	V_{REF}		1.225	1.25	1.275	V
Line regulation	RegLine	V_{CC} = 3V ~ 40V	--	--	6	mV
Total device						
Supply Current	I_{CC}	V_{CC} = 5V ~ 40V, C_T = 1nF, pin7=Vcc, pin5>Vth, pin2=Gnd, remaining pins open	--	3	5	mA

Note: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible

2. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (<=300mA) and high driver currents (>=30mA), it may take up to 2uS for it to come out of saturation. This condition will shorten the off time at frequencies >= 30KHz, and is magnified at high temperature. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

Forced Bata of output switch: **Ic output / (Ic driver – 7mA*) >= 10**

* The 100ohm resistor in the emitter of the driver divide requires about 7mA before the output switch conducts.

TSC

Circuit Description

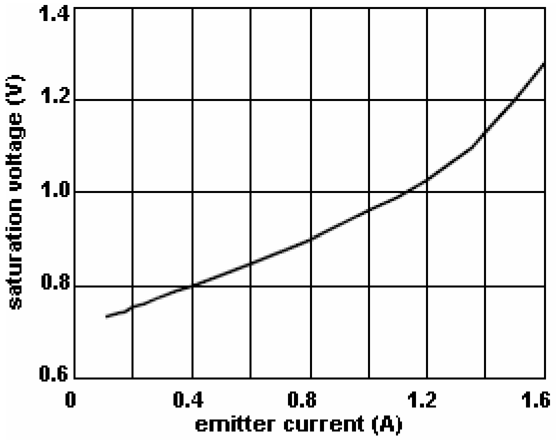


Figure 1. Vce(sat) vs emitter current

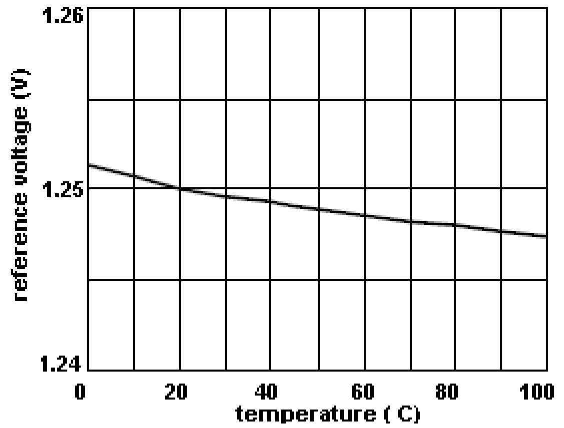


Figure 2. reference voltage vs temp.

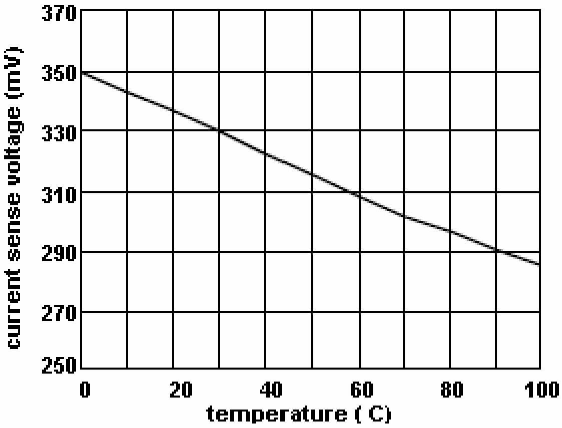


Figure 3. current limit sense voltage vs temperature

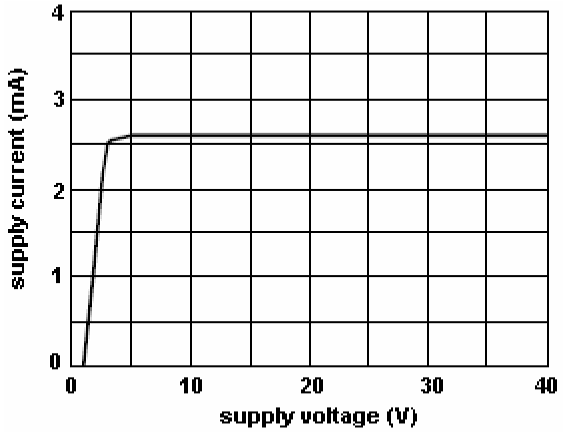


Figure 4. standby supply current vs supply voltage

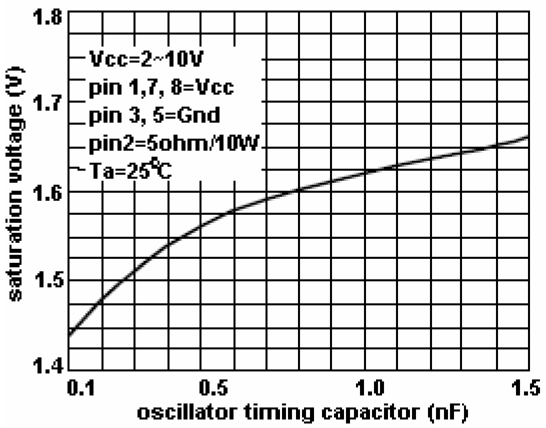


Figure 5. emitter follower configuration output saturation voltage vs emitter current

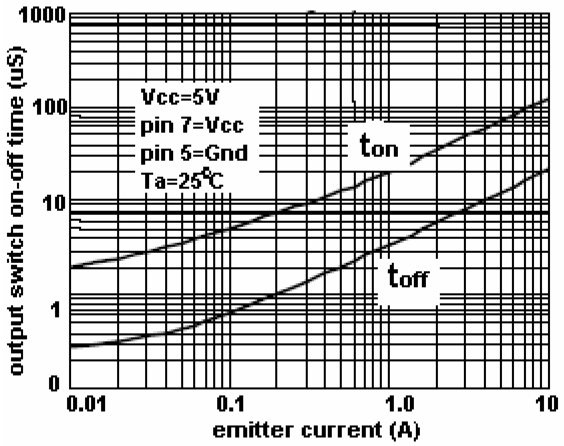


Figure 6. output switch on=off time vs oscillator timing capacitor

Typical Application Circuit

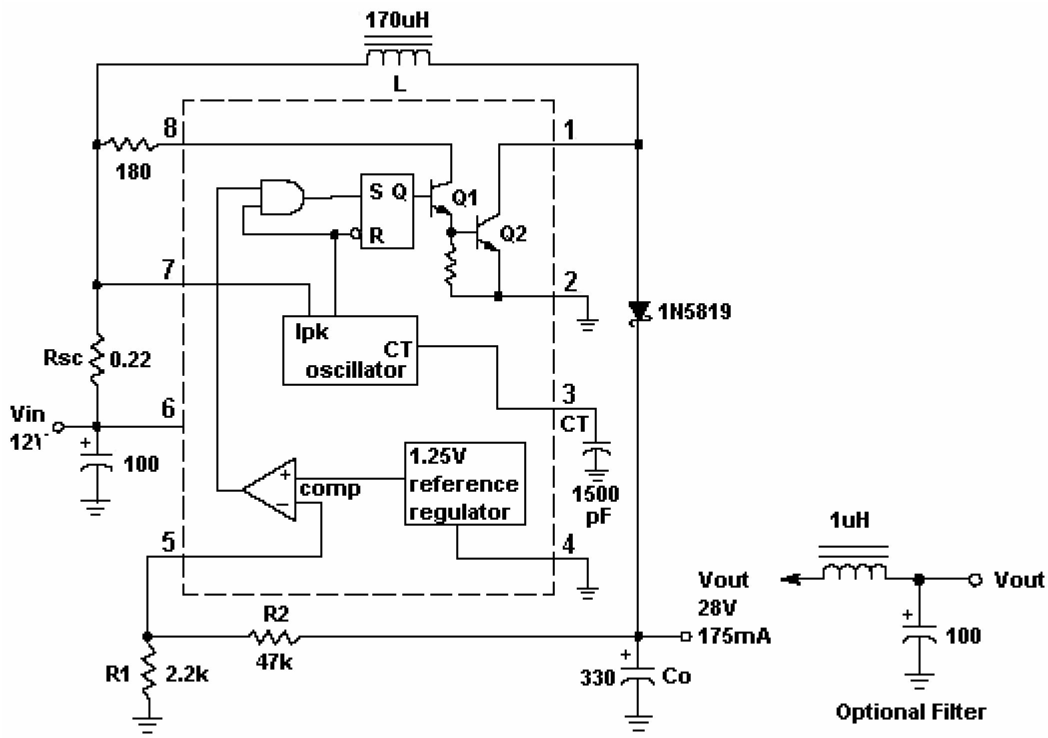


Figure 7. Step Up Converter

Test	Conditions	Results
LINE REGULATION	Vin= 8V~16V, Io= 175mA	30mV +/- 0.05%
Load Regulation	Vin= 12V, Io= 75mA to 175mA	10mV +/- 0.017%
Output Ripple	Vin=12V, Io= 175mA	400mVpp
Efficiency	Vin=12V, Io= 175mA	87.7%
Output Ripple with Optional Filter	Vin=12V, Io= 175mA	40mVpp

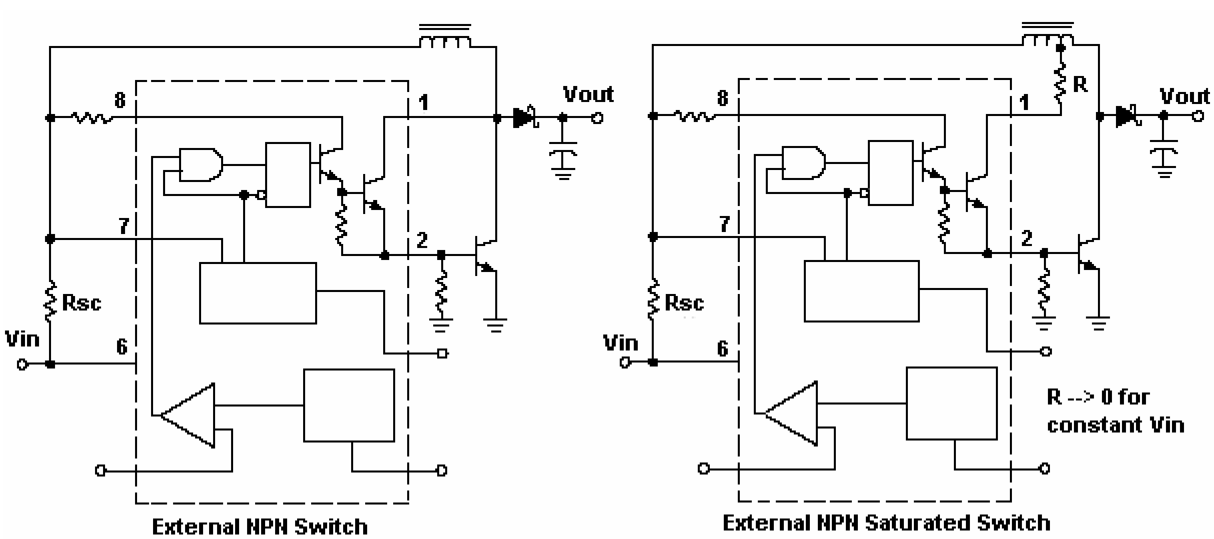


Figure 8. External Current Boost Connections for Ic Peak Greater than 1.5A

Typical Application Circuit (continues)

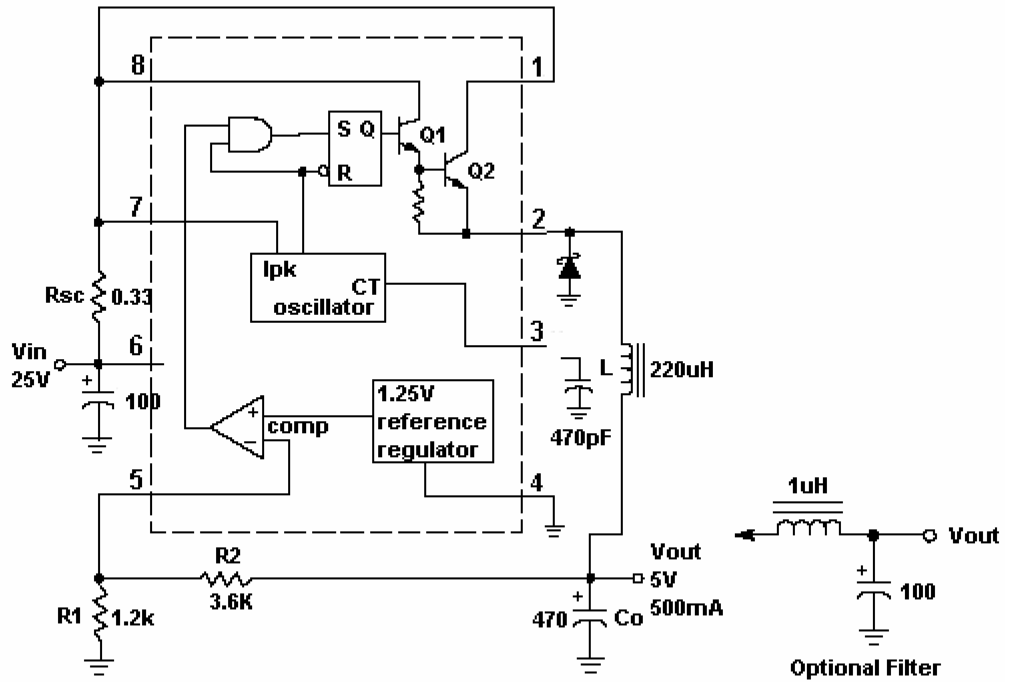


Figure 9. Step Down Converter

Test	Conditions	Results
Line Regulation	Vin= 15V~25V, Io= 500mA	12mV +/- 0.12%
Load Regulation	Vin= 25V, Io= 50mA to 500mA	3mV +/- 0.03%
Output Ripple	Vin= 25V, Io= 500mA	120mVpp
Short Circuit Current	Vin= 25V, RL= 0.1ohm	1.1A
Efficiency	Vin= 25V, Io= 500mA	83.7%
Output Ripple with Optional Filter	Vin= 25V, Io= 500mA	40mVpp

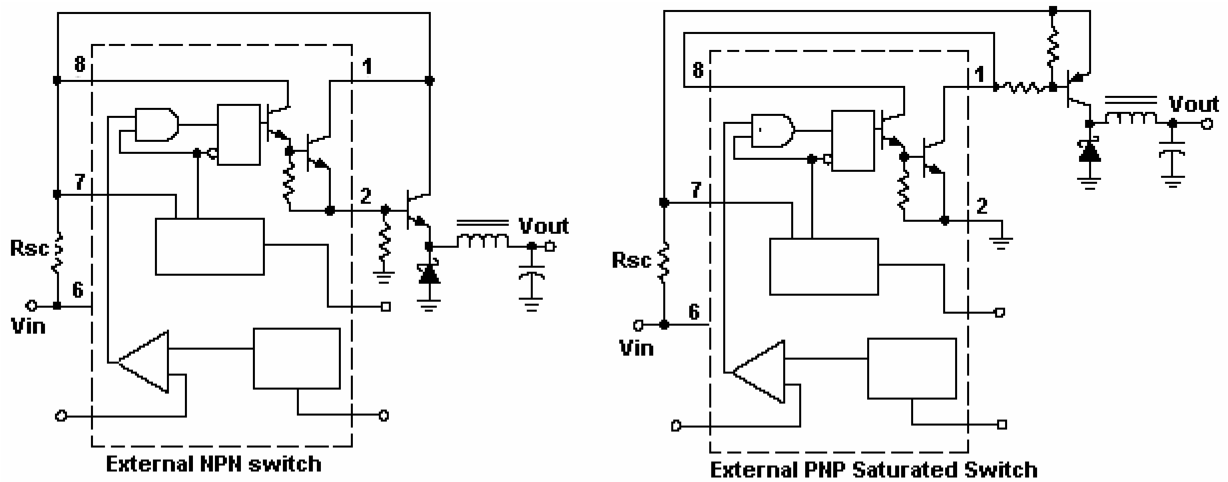


Figure 10. External Current Boost Connections for Ic Peak Greater than 1.5A

Typical Application Circuit (continues)

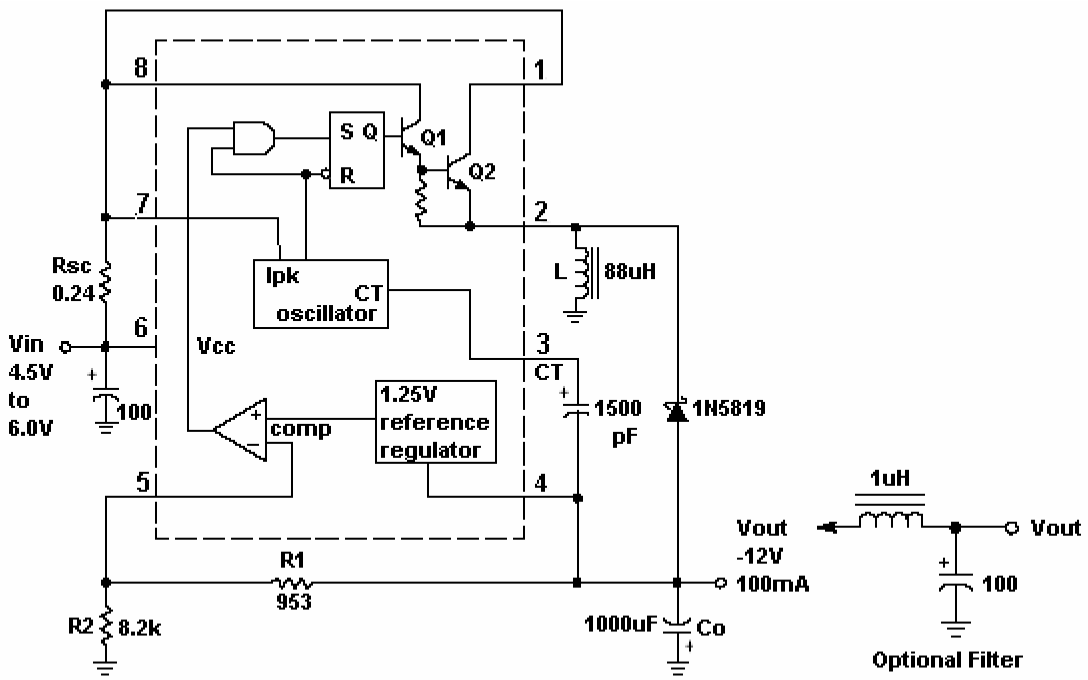


Figure 11. Voltage Inverting Converter

Test	Conditions	Results
Line Regulation	Vin= 4.5V~6.0V, Io= 100mA	3mV +/- 0.012%
Load Regulation	Vin= 5V, Io= 10mA to 100mA	22mV +/- 0.09%
Output Ripple	Vin= 5V, Io= 100mA	500mVpp
Short Circuit Current	Vin= 5V, RL= 0.1ohm	900mA
Efficiency	Vin= 5V, Io= 100mA	62.2%
Output Ripple with Optional Filter	Vin= 5V, Io= 100mA	70mVpp

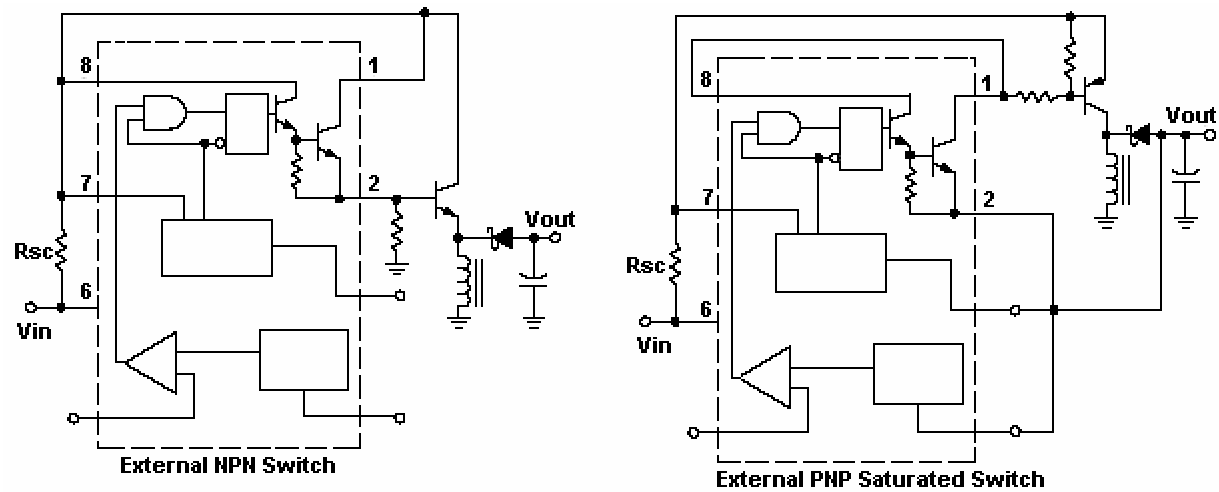


Figure 12. External Current Boost Connections for Ic Peak Greater than 1.5A

Design Formula Table

Test	Step Up	Step Down	Voltage Inverting
ton / toff	$\frac{Vout+Vf-Vin(\min)}{Vcc(\min)-Vsat}$	$\frac{Vout+Vf}{Vcc-Vsat-Vout}$	$\frac{\lvert Vout\rvert+Vf}{Vcc-Vsat}$
(ton+ toff)	$\frac{1}{f\min}$	$\frac{1}{f\min}$	$\frac{1}{f\min}$
CT	$4.0 \times 10^{-5}\ ton$	$4.0 \times 10^{-5}\ ton$	$4.0 \times 10^{-5}\ ton$
Ipk(switch)	$2Iout(max)\left(\frac{ton}{toff}+1\right)$	$2Iout(max)$	$2Iout(max)\left(\frac{ton}{toff}+1\right)$
Rsc	$\left(\frac{0.3}{Ipk(switch)}\right)$	$\left(\frac{0.3}{Ipk(switch)}\right)$	$\left(\frac{0.3}{Ipk(switch)}\right)$
L(min)	$\left(\frac{Vin(\min)-Vsat}{Ipk(switch)}\right)*ton(\max)$	$\left(\frac{Vin(\min)-Vsat-Vout}{Ipk(switch)}\right)*ton(\max)$	$\left(\frac{Vin(\min)-Vsat}{Ipk(switch)}\right)*ton(\max)$
Co	$\left(9\frac{Iout*ton}{Vripple(pp)}\right)$	$\left(\frac{Ipk(switch)(ton+toff)}{8Vripple(pp)}\right)$	$\left(9\frac{Iout*ton}{Vripple(pp)}\right)$

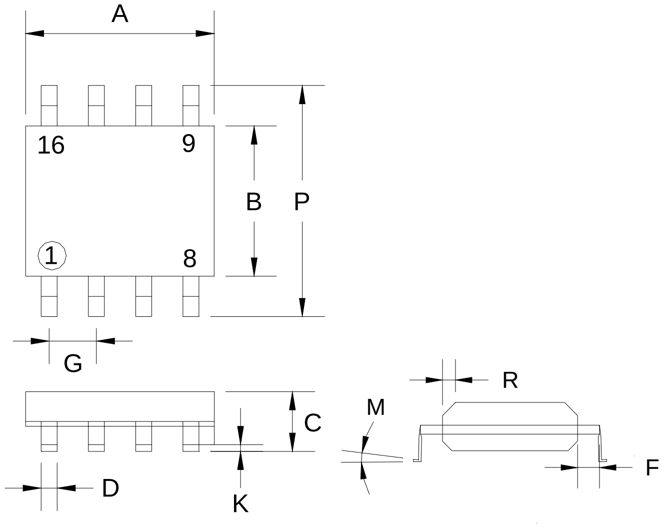
Terms and Definitions

- Vsat = Saturation Voltage of the output switch.
- Vf = Forward Voltage drop of the rectifier.

The following power supply characteristics must be chosen:

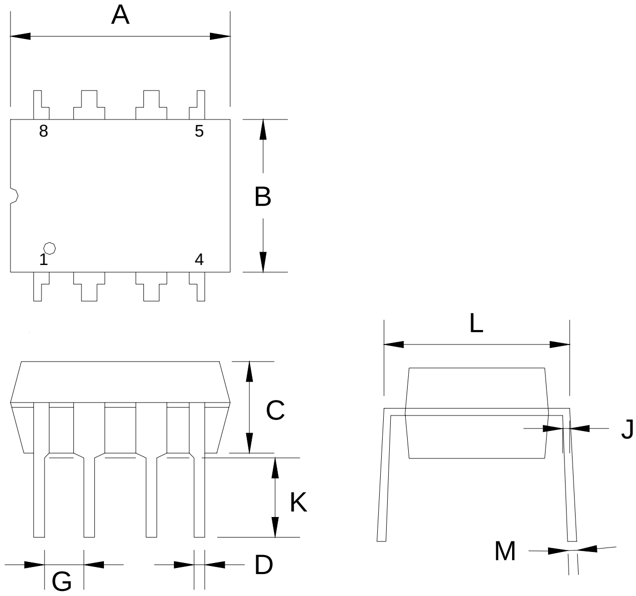
- Vin= Normal input voltage
- Vout: Desied Output voltage, |Vout| =1.25 (1+R2 / R1)
- Iout : Desired output current.
- fmin : Minimum desired output switching frequency at the selected values for Vin and Io.
- Vripple(p-p): Desired peak-to-peak output ripple voltage. in practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 (typ)		0.05 (typ)	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DIP-8 Mechanical Drawing



DIP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	9.32	0.357	0.367
B	6.22	6.48	0.245	0.255
C	3.18	4.45	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54 (typ)		0.10 (typ)	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10°	-	10°